AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An improved high-speed adaptive equalizer device comprising:

one or more controllable analog filters comprising:

one or more data signal inputs for receiving one or more data signals;

one or more control signal inputs for receiving one or more control signals; and

one or more outputs for carrying filtered data signal output signals; and

one or more error generators for assessing the performance of one or more of said controllable analog filters according to one or more error functions coupled to one or more of said analog filters comprising:

one or more inputs for receiving one or more of said filtered data signal output signals from said controllable analog filter, wherein two or more points are assessed across a bit interval using said error functions; and

one or more outputs for carrying error generator output data signals.

2. (Original) The improved high-speed adaptive equalizer device of claim 1 further comprising one or more processing modules for processing said error generator output data signals creating processed data signals.

3. (Original) The improved high-speed adaptive equalizer device of claim 2 wherein one or more of said processing modules comprise one or more error acquisition blocks for applying one or more acquisition filters to one or more of said error generator output data signals thereby creating one or more processed signals coupled to one or more of said error generators comprising:

one or more inputs for receiving said error generator output data signals; and

one or more outputs for carrying processed data signals.

4. (Original) The improved high-speed adaptive equalizer device of claim 3 wherein one or more of said acquisition filters comprise an anti-aliasing filter, a noise reduction filter, a low pass filter or an integrator.

5. (Currently Amended) The improved high-speed adaptive equalizer device of claim 1 further comprising one or more equalizer controllers for controlling one or more of said controllable analog filters according to one or more algorithms comprising:

one or more inputs for receiving equalizer controller input data signals; and

one or more outputs for carrying said control signals coupled to one or more of said control signal inputs.

6. (Original) The improved high-speed adaptive equalizer device of claim 1 wherein said equalizer controller input data signals comprise processed data signals or error generator output data signals.

7. (Original) The improved high-speed adaptive equalizer device of claim 1 wherein said controllable analog filter device comprises a digital, analog or hybrid device.

8. (Original) The improved high-speed adaptive equalizer device of claim 3 wherein one or more of said algorithms comprise a quasi-Newton, steepest descent or multivariate minimization algorithm.

9. (Original) The improved high-speed adaptive equalizer device of claim 1 wherein one or more of said algorithms may be added, updated, activated, decommissioned or deleted.

10. (Original) The improved high-speed adaptive equalizer device of claim 1 wherein one or more of said error functions may be added, updated, activated, decommissioned or deleted.

11. (Original) The improved high-speed adaptive equalizer device of claim 1 wherein said analog filter comprises one or more transversal filters, lattice filters, linear filters or non-linear filters.

12. (Original) The improved high-speed adaptive equalizer device of claim 1 wherein one or more of said data signal inputs comprise analog input, sampled analog input or digital input.

13. (Original) The improved high-speed adaptive equalizer device of claim 1 wherein one or more of said control signal inputs comprise analog input or digital input.

14. (Original) The improved high-speed adaptive equalizer device of claim 1 wherein said equalizer controller comprises one or more processing units, microprocessors, software modules, firmware modules or digital devices.

15. (Original) The improved high-speed adaptive equalizer device of claim 1 wherein said equalizer controller further comprises one or more external data outputs.

16. (Original) The improved high-speed adaptive equalizer device of claim 1 wherein said equalizer controller further comprises one or more external control signal outputs.

17. (Original) The improved high-speed adaptive equalizer device of claim 1 wherein said equalizer controller further comprises one or more external data inputs.

18. (Original) The improved high-speed adaptive equalizer device of claim 1 wherein said equalizer controller further comprises one or more external control signal inputs.

19. (Original) The improved high-speed adaptive equalizer device of claim 1 wherein one or more of said controllable analog filters further comprises one or more external data signal outputs.

20. (Original) The improved high-speed adaptive equalizer device of claim 1 wherein one or more of said error generators further comprises one or more external data signal outputs.

21. (Original) The improved high-speed adaptive equalizer device of claim 1 wherein one or more of said error generators comprises one or more eye monitors.

22. (Original) The improved high-speed adaptive equalizer device of claim 1 wherein one or more of said error generators comprises a clock or clock recovery system.

23. (Original) The improved high-speed adaptive equalizer device of claim 1 wherein one or more of said error generators is coupled to a clock or clock recovery system.

24. (Original) The improved high-speed adaptive equalizer device of claim 1 wherein one or more of said error generators comprises one or more weighting function modules.

25. (Original) The improved high-speed adaptive equalizer device of claim 1 further comprising one or more modules comprising a capacity reporting module, a device status module, a link monitor or a monitoring module.

26. (Original) The improved high-speed adaptive equalizer device of claim 1 further comprising one or more modules comprising a joint optimization module, a chromatic dispersion module, a receiver gain module, a sampling phase module, a decision threshold level module or a DC offset module.

27. (Currently Amended) A method for improved high-speed adaptive equalization, said method comprising ~~the steps of~~:

receiving one or more data inputs at one or more controllable analog filters;

filtering said one or more data inputs according to filter coefficients to create one or more filtered data signals;

receiving said filtered data signals at one or more error generators; and

assessing the performance of one or more of said controllable analog filters according to one or more error functions creating one or more error generator output data signals, wherein two or more points are assessed across a bit interval using said error functions.

28. (Currently Amended) The method of claim 27 further comprising ~~the step of~~ providing one or more external data output signals after the step of filtering.

29. (Currently Amended) The method of claim 27 wherein said ~~the step of~~ assessing the performance of one or more of said controllable analog filters further comprises applying a function to said filtered data signals comprising a normalization function or level shift function.

30. (Currently Amended) The method of claim 27 wherein said ~~the step of~~ assessing the performance of one or more of said controllable analog filters further comprises applying one or more weighting functions to said error generator output data signals.

31. (Currently Amended) The method of claim 27 further comprising ~~the step of~~ processing said error generator output signals creating processed data signals.

32. (Currently Amended) The method of claim 31 wherein said ~~the step of~~ processing said error generator output signals comprises ~~the steps of~~:

receiving said error generator output data signals at an error acquisition module; and

filtering said error generator output data signals according to one or more acquisition filters.

33. (Currently Amended) The method of claim 32 wherein said ~~the step of~~ filtering said error generator output data signals according to one or more acquisition filters comprises ~~the step of~~ processing said error generator

output data signals with a filter comprising an anti-aliasing filter, a nose reduction filter, a low pass filter or an integrator.

34. (Currently Amended) The method of claim 32 further comprising ~~the step of~~ digitizing said error generator output data signals.

35. (Currently Amended) The method of claim 27 further comprising ~~the steps of~~:

receiving equalizer controller input data signals at an equalizer controller;

computing a new set of filter coefficients according to one or more error minimization algorithms; and

controlling one or more of said controllable analog filters by adjusting said filter coefficients to said new set of filter coefficients.

36. (Original) The method of claim 35 wherein said equalizer controller input data signals comprise processed data signals or error generator output data signals.

37. (Currently Amended) The method of claim 35 further comprising ~~the step of~~ executing joint optimization with respect to one or more external devices.

38. (Currently Amended) The method of claim 35 further comprising ~~the step of~~ assessing capacity, device status or link monitor status based on said filter coefficients.

39. (Currently Amended) The method of claim 38 further comprising ~~the step of~~ reporting said capacity, device status or link monitor status based on said filter coefficients.

40. (Currently Amended) The method of claim 27 further comprising ~~the step of~~ operating iteratively.

41. (Currently Amended) The method of claim 27 further comprising ~~the step of~~ initializing one or more of said controllable analog filters to an initial setting comprising a set of said filter coefficients based on a pass-through mode, stored values or external input.

42. (Currently Amended) A system for improved optical networking comprising:

an improved high-speed adaptive equalizer device comprising:

one or more controllable analog filters comprising:

one or more data signal inputs for receiving one or more data signals;

one or more control signal inputs for receiving one or more control signals; and

one or more outputs for carrying filtered data signal output signals; and

one or more error generators for assessing the performance of one or more of said controllable analog filters according to one or more error functions coupled to one or more of said analog filters comprising:

one or more inputs for receiving one or more of said filtered data signal output signals from said controllable analog filter, wherein two or more points are assessed across a bit interval using said error functions; and

one or more outputs for carrying error generator output data signals.

43. (Original) The system of claim 42 wherein said improved high-speed adaptive equalizer further comprises one or more processing modules for processing said error generator output data signals creating processed data signals.

44. (Original) The system of claim 43 wherein one or more of said processing modules comprise one or more error acquisition blocks for applying one or more acquisition filters to one or more of said error generator output data signals thereby creating one or more processed signals coupled to one or more of said error generators comprising:

one or more inputs for receiving said error generator output data signals; and

one or more outputs for carrying processed data signals.

45. (Currently Amended) The system ~~improved high-speed adaptive equalizer device~~ of claim 44 wherein one or more of said acquisition filters comprise an anti-aliasing filter, a noise reduction filter, a low pass filter or an integrator.

46. (Currently Amended) The system of claim 42 wherein said improved high-speed adaptive equalizer further comprises one or more equalizer controllers for controlling one or more of said controllable analog filters according to one or more algorithms comprising:

one or more inputs for receiving equalizer controller input data signals; and

one or more outputs for carrying said control signals coupled to one or more of said control signal inputs.

47. (Original) The system of claim 42 wherein said equalizer controller input data signals comprise processed data signals or error generator output data signals.

48. (Original) The system of claim 42 wherein said controllable analog filter device comprises a digital, analog or hybrid device.

49. (Original) The system of claim 44 wherein one or more of said algorithms comprise a quasi-Newton, steepest descent or multivariate minimization algorithm.

50. (Original) The system of claim 42 wherein one or more of said algorithms may be added, updated, activated, decommissioned or deleted.

51. (Original) The system of claim 42 wherein one or more of said error functions may be added, updated, activated, decommissioned or deleted.

52. (Original) The system of claim 42 wherein said analog filter comprises one or more transversal filters, lattice filters, linear filters or non-linear filters.

53. (Original) The system of claim 42 wherein one or more of said data signal inputs comprise analog input, sampled analog input or digital input.

54. (Original) The system of claim 42 wherein one or more of said control signal inputs comprise analog input or digital input.

55. (Original) The system of claim 42 wherein said equalizer controller comprises one or more processing units, microprocessors, software modules, firmware modules or digital devices.

56. (Original) The system of claim 42 wherein said equalizer controller further comprises one or more external data outputs.

57. (Original) The system of claim 42 wherein said equalizer controller further comprises one or more external control signal outputs.

58. (Original) The system of claim 42 wherein said equalizer controller further comprises one or more external data inputs.

59. (Original) The system of claim 42 wherein said equalizer controller further comprises one or more external control signal inputs.

60. (Original) The system of claim 42 wherein one or more of said controllable analog filters further comprises one or more external data signal outputs.

61. (Original) The system of claim 42 wherein one or more of said error generators further comprises one or more external data signal outputs.

62. (Original) The system of claim 42 wherein one or more of said error generators comprises one or more eye monitors.

63. (Original) The system of claim 42 wherein one or more of said error generators comprises a clock or clock recovery system.

64. (Original) The system of claim 42 wherein one or more of said error generators is coupled to a clock or clock recovery system.

65. (Original) The system of claim 42 wherein one or more of said error generators comprises one or more weighting function modules.

66. (Original) The system of claim 42 wherein said improved high-speed adaptive equalizer device further comprises one or more modules comprising a capacity reporting module, a device status module, a link monitor or a monitoring module.

67. (Original) The system of claim 42 wherein said improved high-speed adaptive equalizer device further comprises one or more modules comprising a joint optimization module, a chromatic dispersion module, a receiver gain module, a sampling phase module, a decision threshold level module or a DC offset module.